

Enroll No

K.E.Society's
Rajarambapu Institute of Technology, Rajaramnagar
 (An Empowered Autonomous Institute, Affiliated to SUK)
 End Semester Examination 2025-26-I (Jan. 2026)
 F.Y.B.C.A. SEM I

Q.P.Code
E1527

Course Code: BC127

Course Name: Computer Architecture

Day & Date: Friday 16.11.2026

Time : 2:15 To 5:15

Max Marks: 100

- Instructions:**
- 1) All questions are compulsory.
 - 2) Figures in rounded() brackets within the question, indicate the scheme of marking for respective part of the question, whereas, figures in the first right column indicate total marks for that whole question.
 - 3) CO is the index number of the Course Outcome statement.
 - 4) The Bloom's taxonomy level (BL) for 1,2,3,4,5 and 6 is remember, understand, apply, analyze, evaluate and create respectively.
 - 5) Assume suitable data if necessary.
 - 6) Use of non-programmable calculators is allowed

	Marks	COs	BT Level
Q.1 Attempt both parts (a) and (b) of Question	15		
(a) Explain digital and analog signals(4M) and differentiate between them by listing any three differences. (3M)	7	1	2
(b) Apply the Karnaugh Map (K-Map) method to solve the following Boolean functions using the SOP (Sum of Products) form:	8	1	3
a) $F(A, B, C) = \Sigma(0, 2, 4, 6)$ (4M)			
b) $F(A, B, C, D) = \Sigma(1, 3, 4, 5, 9, 11, 12, 13)$ (4M)			
OR			
(b) Analyze any two Boolean laws and show how their truth tables support each law. (each law has 4M)	8	1	4
Q.2 Attempt both parts (a) and (b) of Question	15		
(a) Apply your knowledge of adders to do the following:			
a) Construct the truth tables for Half Adder and Full Adder. (2M)			
b) Write the Sum and Carry expressions for each adder. (2M)	8	1	3
c) Draw the block diagrams of Half Adder and Full Adder. (2M)			
d) Draw the logic circuit diagrams for both adders using basic logic gates. (2M)			

OR



(a) Apply your knowledge of subtractors to do the following:			
a) Construct the truth tables for Half Subtractor and Full Subtractor. (2M)			
b) Write the Difference and Borrow expressions for each subtractor. (2M)	8	1	3
c) Draw the block diagrams of Half Subtractor and Full Subtractor. (2M)			
d) Draw the logic circuit diagrams for both subtractors using basic logic gates. (2M)			
(b) Analyze encoder and decoder by drawing their diagrams and explaining the flow of inputs and outputs in each case. (7M)	7	1	4
Q.3 Attempt both parts (a) and (b) of Question	15		
(a) Analyze shift registers and list their types.	7	1	4
OR			
(a) Analyze counters by listing their types and applications.	7	1	4
(b) Explain the following flip-flops with their definitions, truth tables, and logic diagrams:			
1. SR Flip-Flop (2M)			
2. JK Flip-Flop (2M)	8	1	3
3. D Flip-Flop (2M)			
4. T Flip-Flop (2M)			
Q.4 Attempt both parts (a) and (b) of Question	15		
(a) Apply your knowledge of instruction code and identify the opcode and operand (7M)	7	2	3
(b) Explain Memory-Reference Instructions with instruction formats. (8M)	8	2	3
OR			
(b) Explain the Instruction Cycle (CPU Cycle) in detail. (8M)	8	2	3
Q.5 Attempt any 2 of the following questions	20Marks		
(a) Analyze the concept of Parallel Processing by explaining its basic working mechanism and discussing the different types and levels of parallelism used in computer systems. (10M)	10	3	4
(b) Examine peripheral devices by classifying them into their major types and explaining the purpose of each type. (10M)	10	3	4
(c) Explain the concept of pipelining in a CPU. (10M)	10	3	4
Q.6 Attempt any 2 of the following questions	20Marks		
(a) Examine the memory hierarchy in a computer system by classifying its levels and explaining the purpose of each level. (10M)	10	4	4
(b) Analyze memory management hardware by explaining its components and how address translation works in a computer system. (10M)	10	4	4
(c) Explain auxiliary memory and associative memory. (10M)	10	4	2

